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HIGH PERFORMANCE EMBEDDED DRAM TECHNOLOGY WITH STRAINED SILICON

FIELD OF THE INVENTION

The field of the invention is semiconductor processing. Specifically, the invention relates to forming semiconductor devices in a strained layer region and a strained layer-free region of the same substrate.

BACKGROUND OF THE INVENTION

Semiconductor devices such as Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET's) formed on strained silicon channels have been shown to offer dramatic improvements in mobility and performance. The successful integration of high-performance strained silicon logic type MOSFET's with memory such as dense, low-leakage Dynamic Random Access Memory (DRAM) arrays on the same semiconductor chip for embedded-DRAM applications has not been achieved due to the need to maintain high quality, defect-free silicon in the DRAM array areas while providing strained silicon in the logic support areas. Strained silicon and the substrate required to produce the strain inherently results in greatly increased silicon dislocations, which makes it incompatible with low-leakage DRAM cells. Furthermore, semiconductor processes which exceed certain temperatures that are required for the DRAM cell formation may be incompatible with currently practiced strained silicon formation.

Forming high-performance strained silicon support MOSFETs on the same substrate with

low-leakage high-density DRAM cells is desired.

SUMMARY OF THE INVENTION

It is thus an object of the present invention to form high-performance strained silicon support MOSFETs on the same substrate with low-leakage high-density DRAM cells.

The present invention discloses a first semiconductor device such as, for example, a low-leakage DRAM cell, formed in a strained layer-free region of a semiconductor substrate. On the same semiconductor substrate, a strained layer region is selectively formed in the semiconductor substrate separate from the strained layer-free region and a second semiconductor device such as, for example, a high-performance MOSFET, is formed in the strained layer region.

DESCRIPTION OF THE DRAWING

The foregoing and other features of the invention will become more apparent upon review of the detailed description of the invention as rendered below. In the description to follow, reference will be made to the several figures of the accompanying Drawing, in which:

FIGS. 1-8 are cross sectional views of the semiconductor structure as it appears during the steps according to the method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

Referring to FIG. 1, p-type silicon substrate 10 is provided having memory cell 12 formed in a strained layer-free region of substrate 10. In FIG. 1, memory cell 12 is a DRAM cell having a trench storage capacitor 14 and vertical MOSFET 16, which can be formed, for example, as described in commonly assigned U.S. Patent No. 6,225,158 B1, herein incorporated by reference. Although memory cell 12 is shown in FIG. 1 as having a trench storage capacitor 14 and vertical MOSFET 16, it should be noted that memory cell 12 can be formed using other types of capacitors and FET's such as a stacked capacitor or a planar MOSFET. In this example, trench storage capacitor 14 includes: deep trench 18, n+ buried plate 20, nitride/oxide node dielectric 22, n+ polysilicon 24 and 26, collar oxide 28 and n+ buried strap diffusion 30. Further, vertical MOSFET 16 includes: trench top oxide 32, gate oxide 34 formed on the sidewalls of deep trench 18, and n+ polysilicon gate conductor 36. It should be noted that two memory cells 12 are shown in the array region throughout FIGS. 1-8. However, it should be understood that any number of one or more memory cells 12 can be formed in the array region.

After formation of memory cells 12 in strained layer-free regions of substrate 10, strained layer regions are formed in substrate 10 for the subsequent formation of high performance MOSFETS. Thus, process incompatibilities such as high temperatures used in the formation of the memory cells are avoided since the strained layer regions and the MOSFETS are formed after the memory cells are formed.

A thin layer 40 (e.g. silicon oxide) is deposited on pad film 38 (which can include, for example, a pad nitride and a pad oxide layer) and exposed portions of gate conductor 36 as shown in FIG. 2. Oxide layer 40 serves as an etch stop layer in subsequent processing.

Another layer 42 (e.g. silicon nitride) is then deposited on oxide layer 40, and a hard mask layer 44 (e.g. silicon oxide) is deposited on silicon nitride layer 42.

A block resist (not shown) is patterned on oxide hard mask layer 44 and a reactive ion etch is used to etch through exposed portions of layers 38, 40, 42,44 and into substrate 10 to a preferred depth of about 100nm to about 400nm, more preferably about 200nm, to form trench 46 as shown in FIG. 2. Any remaining block resist is removed from oxide hard mask layer 44 after the formation of trench 46.

Referring to FIG. 3, oxide hard mask layer 44 is removed by a standard process, such as reactive ion etching selective to silicon nitride layer 42 and silicon exposed by trench 46. Spacer 48 comprising a material upon which silicon or Silicon Germanium (SiGe) will not nucleate, such as silicon oxide or nitride, is formed on sidewall surface 50 of trench 46, such as by conventional deposition and RIE. A linear graded buffer layer technique can be used to grow SiGe layer 52 with low dislocation density (~10^5 cm-2) in trench 46. Growth conditions are favored to selectively form SiGe layer 52 on substrate 10, and not on spacer 48. Preferably, SiGe layer 52 is epitaxially grown upward from exposed bottom surface 54 of trench 46 until SiGe layer 52 is above the top surface of silicon nitride layer 42. Overgrown SiGe layer 52 is planarized to the top surface of silicon nitride layer 42 by a process such as chemical mechanical polishing (CMP). Silicon CMP processes that are known in the art can be used to planarize SiGe layer 52.

Optionally, spacer 48 can be omitted, however, spacer 48 prevents SiGe layer 52 from nucleating and epitaxially growing outward from sidewall surface 50 resulting in two growth fronts in SiGe layer 52. In addition, spacer 48 isolates strain produced by SiGe layer 52 in substrate 10 to the supports area of the chip, thus isolating the storage capacitor cells in the array from the strain.

Next, upper surface 56 of SiGe layer 52 is selectively recessed by an etch process such as a reactive ion etch using an SF6 gas or an oxidation followed by an HF wet etch to a depth below the upper surface of silicon nitride layer 42, as shown in FIG. 4. Optionally, the recess of SiGe layer 52 may be omitted, since the subsequently grown strained layer is very thin.

Referring to FIG. 5, a thin layer of epitaxial silicon 58 is selectively grown on upper surface 56 of SiGe layer 52. Epitaxial silicon layer 58 is grown to a thickness preferably less than about 50 nm, more preferably from about 2.5 nm to about 10 nm. Due to the lattice mismatch between SiGe layer 52 and thin epitaxial silicon layer 58, epitaxial silicon layer 58 undergoes a tensile lattice strain which enhances the mobility of subsequently formed FETs. After the growth of epitaxial silicon layer 58, silicon nitride layer 42 is removed selective to oxide layer 40 and epitaxial silicon layer 58 by processes known in the art, such as a wet etch comprising hot phosphoric acid. It should be noted that strained layer 58 can also be formed by other methods such as, for example, depositing titanium (Ti) or Cobalt (Co) metal on upper surface 56 of SiGe layer 52 and forming a thin layer of titanium silicide or cobalt silicide. Another example of forming strained layer 58 includes implanting into upper surface 56 of SiGe layer 52 an element having a lattice constant different than SiGe such as, for example, carbon (C) or germanium (Ge).

Referring to FIG. 6, a silicon nitride layer 60 is deposited on oxide layer 40 and strained silicon layer 58, and it is then patterned to expose the supports while the arrays remain covered. The active areas in the supports are patterned to form shallow trench isolations (STI) 62, that are filled using known methods, such as TEOS CVD oxide or HDP oxide, followed by planarizing. Sacrificial oxide (not shown) is grown in the supports and well implants (not shown) are formed . Sacrificial oxide is removed and support gate

dielectric 64 is formed on strained silicon layer 58 by growing a thin dielectric film, such as thermal oxide or nitrided oxide. Support gate conductor 66 is formed in the strained layer region (supports), and portions of gate conductor 66 remaining in the strained layer region (array) are removed using a block mask.

Referring to FIG. 7, silicon nitride layer 60 is removed from the array selective to oxide layer 40 by methods known in the art, such as a wet etch comprising hot phosphoric acid. Oxide layer 40 is then removed selective to silicon nitride layer 38. Wordline conductor 68, such as tungsten/tungsten silicide, and cap layer such as silicon nitride 70, are deposited in the support and array regions.

Referring to FIG. 8, support gate 66, wordlines 68 and cap layer 70 are simultaneously patterned and etched with a common mask. Optionally, two masks could be used to form support gate 66 and wordlines 68. For example, one mask could be used to form support gate 66 while another mask could be used to form wordlines 68 in order to individually optimize specific properties of each, such as linewidth for performance considerations.

Standard processing follows, which includes: support S/D extension, halo and contact implants; gate sidewall oxidation to heal any damage due to gate etch; spacer formation; support and bitline contact studs; interlevel dielectrics; and, deposition and patterning of upper layers of wiring, including bitline conductors.

Additionally, if propagation of silicon dislocations from the strained layer SiGe region into the strained layer-free memory array is a concern, dummy deep storage trenches may be used as a buffer between the strained layer (supports) and the strained layer-free (array) regions.

While the invention has been described above with reference to the preferred embodiments thereof, it is to be understood that the spirit and scope of the invention is not limited thereby. Rather, various modifications may be made to the invention as described above without departing from the overall scope of the invention as described above and as set forth in the several claims appended hereto.